CLAIMS

What is claimed is:

1. An equalization circuit, comprising:

a first sense amplifier having an input, the input being electrically isolated from an input to a second sense amplifier;

an equalizer connected to the input to the first sense amplifier to provide an equalizing voltage to the input to the first sense amplifier; and

wherein the input to the first sense amplifier may be equalized by the equalizing voltage independent from the input to the second sense amplifier.

2. The equalization circuit set forth in claim 1, wherein the input to the first sense amplifier is electrically isolated from the input to the second sense amplifier by a capacitor.

3. The equalization circuit set forth in claim 1, wherein the input to the first sense amplifier comprises a bitline of a memory device.

4. A sense amplifier circuit, comprising:

a first sense amplifier having an input coupled to a long bitline;

a second sense amplifier having an input coupled to a short bitline, the input to the second sense amplifier being electrically isolated from the input to the first sense amplifier;

an equalizer connected to the input to the first sense amplifier to provide an equalizing voltage thereto;

an equalizer connected to the input of the second sense amplifier to provide an equalizing voltage thereto; and

wherein the input to the second sense amplifier may be equalized by the equalizing voltage from the second equalizer independent from the equalizing voltage from the first equalizer.

5. The sense amplifier circuit set forth in claim 4, wherein the input to the first sense amplifier is electrically isolated from the input to the second sense amplifier by a capacitor.

6. An integrated circuit device, comprising:

a memory array having a plurality of memory cells;

a first signal path that provides access to the plurality of memory cells;

a first sense amplifier connected to the first signal path, the first signal path being electrically isolated from a second signal path; and

an equalizer connected to the first signal path to provide an equalizing voltage to the first signal path, wherein the first signal path may be equalized by the equalizing voltage independent from a voltage on the second signal path.

7. The integrated circuit device set forth in claim 6, wherein the first signal path is electrically isolated from the second signal path by a capacitor.

8. The integrated circuit device set forth in claim 6, wherein the first signal path comprises a bitline.

9. The integrated circuit device set forth in claim 6, comprising an equalizer coupled to the second signal path to provide an equalizing voltage to the second signal path.

10. An electronic device, comprising:

a processor adapted to execute instructions;

a storage device adapted to store instructions to be executed by the processor; and

a memory device that receives information stored on the storage device, the memory device comprising:

a memory array that includes a plurality of memory cells;

a first signal path that provides access to the plurality of memory cells;

a first sense amplifier connected to the first signal path, the first signal path being electrically isolated from a second signal path; and

an equalizer connected to the first signal path to provide an equalizing voltage to the first signal path, wherein the first signal path may be equalized by the equalizing voltage independent from a voltage on the second signal path.

11. The electronic device set forth in claim 10, wherein the first signal path is electrically isolated from the second signal path by a capacitor.

12. The electronic device set forth in claim 10, wherein the first signal path comprises a bitline.

13. The electronic device set forth in claim 10, comprising an equalizer coupled to the second signal path to provide an equalizing voltage to the second signal path.

14. The electronic device set forth in claim 10, comprising a user input device adapted to receive data for use by the processor.

15. The electronic device set forth in claim 10, comprising a display device adapted to produce an image for viewing by a user based on instructions executed by the processor.

16. A method of accessing a memory device, comprising:

storing data in a memory cell associated with a sense amplifier circuit;

equalizing a first bitline segment associated with the sense amplifier in isolation from a second bitline segment; and

reading data from the memory cell via the sense amplifier circuit.

17. The method set forth in claim 16, wherein the recited acts are performed in the recited order.

18. A method of producing a memory device, the method comprising:

providing a sense amplifier circuit; and electrically isolating a bitline connected to the sense amplifier circuit from a second bitline.

19. The method set forth in claim 18, wherein the act of electrically isolating the bitline comprises capacitively coupling the bitline to the second bitline.

20. The method set forth in claim 18, wherein the recited acts are performed in the recited order.